Advantages of FLEX 8000 I/O Timing

TECHNICAL BRIEF 11 APRIL 1997

The speed at which a signal enters and exits a device can significantly impact overall system performance. Predictable I/O timing is important because it allows system designers to select a device in advance, knowing the device will be able to interface with the other devices on the printed circuit board independent of device routing. FLEX 8000 I/O cell registers have a predictable, fast clock-to-output delay (t_{CO}), which plays a critical role in maximizing inter-device performance. In contrast, segmented FPGAs that do not have I/O cell registers force designers to use registers from the internal logic array for all I/O interfacing, resulting in slow, unpredictable I/O performance.

I/O Cell Registers Provide Output Delay Predictability

For a specific speed grade, the FLEX 8000 t_{CO} delay is constant, regardless of device utilization or logic placement. In contrast, the lack of I/O cell registers in some FPGAs magnifies the unpredictability inherent in their segmented architecture. The length of the path between any two points in a segmented architecture is a function of the number of routing resources available in the device. As device utilization increases, there is a higher probability that a signal will be forced to take an indirect path. To obtain the best-case t_{CO} performance for FPGAs that do not have I/O cell registers, designers must manually select the specific cell that is closest to the I/O pin. If this optimal placement is not possible due to routing limitations, I/O timing can vary dramatically depending on the cell and routing path available. Even if the designer has access to long lines, the t_{CO} for the FPGA can vary by over 100%. This variance can be even greater as long line resources become limited in the device.

I/O Registers Provide Superior Output Performance

The clock-to-output time (t_{CO}) is the critical parameter that impacts output performance. The FLEX 8000 device I/O cell register provides a consistently fast t_{CO}. For example, the I/O cell register for a FLEX 8000A device in a -4 speed grade has a t_{CO} of 10.1 ns (see Table 1). According to tests performed by Altera, this speed is 76% faster than the 17.8-ns t_{CO} of the best-case condition (i.e., closest cell to the I/O pin) for the Xilinx XC5210-5 device, which does not have I/O cell registers. For even higher output performance, designers can use a FLEX 8000A device in a -2 speed grade to obtain an 8.8-ns t_{CO}.

Table 1. Device Output Timing Comparison[1]

Parameter	Altera EPF81188A (ns)		Xilinx XC5210-5 (ns)		
	A-4	A-2	Closest Cell[2]	Mid Cell[3]	Worst Cell[4]
Clock to output (t_{CO})	10.1	8.8	17.8	28.9	36.1

[1] Data is based on tests performed by Altera
[2] Cell directly adjacent to I/O pin
[3] Cell in center of device connected to I/O pin via long lines
[4] Cell at opposite corner of device connected to I/O pin via long lines

FastTrack Interconnect Provides Input Predictability

For input timing, the set-up time (t_{SU}) and hold time (t_H) are the critical parameters. The I/O blocks for the Xilinx XC5210-5 device contain a programmable delay in the input path that effectively provides a zero hold time for internal cells used as input registers (see Table 2).

Table 2: XC5210-5 Device Input Timing[1]

Parameter	XC5210-5 Internal Cell (ns)		
	Closest Cell[1]	Mid Cell[2]	Worst Cell[3]
Setup time with delay (t_{SU})	2.7	9.4	13.9
Hold time with delay (t_H)	0.0	0.0	0.0

[1] Data is based on tests performed by Altera
[2] Cell directly adjacent to I/O pin
[3] Cell in center of device connected to I/O pin via long lines
[4] Cell at opposite corner of device connected to I/O pin via long lines

This programmable delay and resulting 0-ns hold time is positioned as an advantage over FLEX 8000 devices, which have I/O cell registers with positive input hold times. However, FLEX 8000 core registers—which have a guaranteed pin-to-pin t_H of zero—can be used as input registers. These core registers combined with the FastTrack Interconnect give FLEX 8000 devices superior input timing predictability (see Table 3). While the set-up time for a FLEX 8000 core register varies by only 0.4 ns, the set-up time for an XC5210-5 device can vary by up to 11.2 ns.

Table 3: FLEX 8000 Device Input Timing

Parameter	EPF81188A-4 Internal Cell (ns)			EPF81188A-2 Internal Cell (ns)		
	Closest Cell[1]	Mid Cell[2]	Worst Cell[3]	Closest Cell[1]	Mid Cell[2]	Worst Cell[3]
Setup time (t_{SU})	3.6	3.8	4.0	2.3	2.5	2.7
Hold time (t_H)	0.0	0.0	0.0	0.0	0.0	0.0

[1] Cell directly adjacent to I/O pin
[2] Cell in center of device connected to I/O pin
[3] Cell at opposite corner of device connected to I/O pin

FLEX 8000 Provides Predictable Performance

I/O cell registers give FLEX 8000 devices faster and more predictable output timing than that available in FPGAs that do not have I/O cell registers. In addition, when using core registers as input registers, the FastTrack Interconnect provides superior input predictability.

The documents listed below provide more detailed information. Part numbers are in parentheses.

Data Sheets

FLEX 8000 Programmable Logic Device Family Data Sheet *(A-DS-F8000-08)*

Application Notes

AN 76 *Understanding FLEX 8000 Timing (A-AN-076-01)*

You can request these documents from:

- Altera Express fax service at (800) 5-ALTERA
- World-wide web at **http://www.altera.com**
- Your local Altera sales representative